EE105
Microelectronic Devices and Circuits

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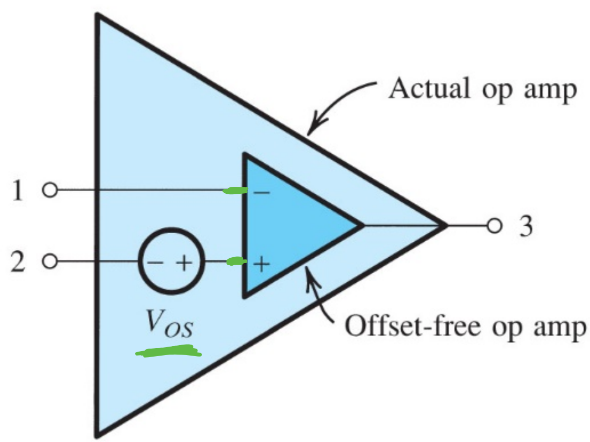
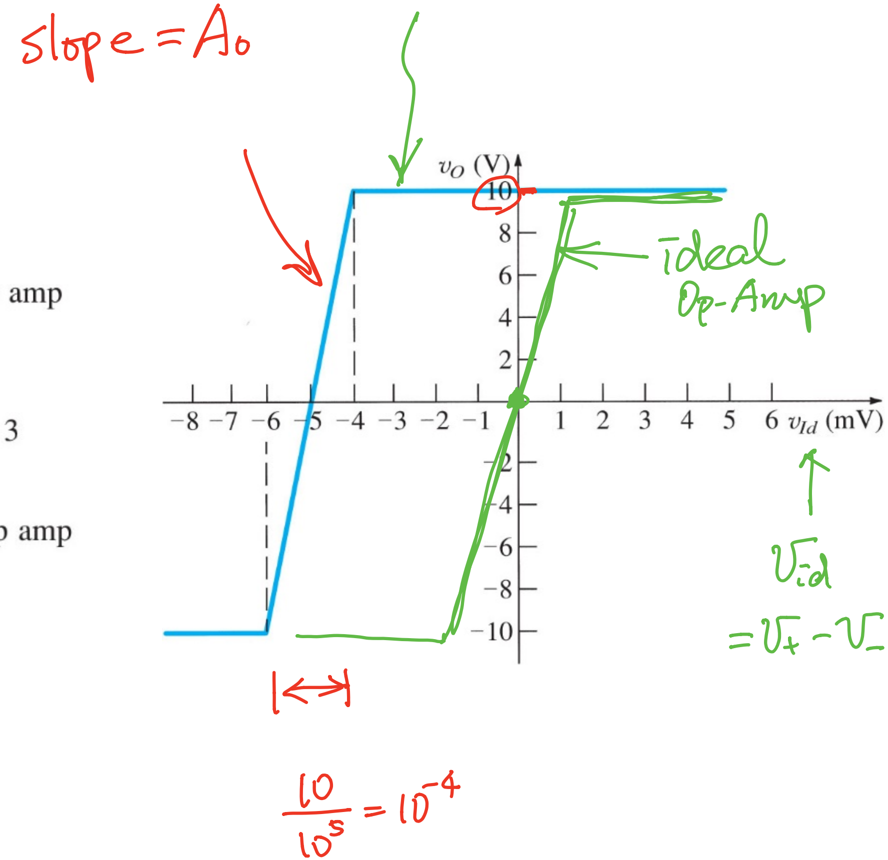
Practical Op-Amps

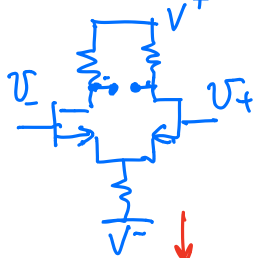
- Linear Imperfections:
  - Finite open-loop gain ($A_0 < \infty$)
  - Finite input resistance ($R_i < \infty$)
  - Non-zero output resistance ($R_o > 0$)
  - Finite bandwidth / Gain-BW Trade-off
- Other (non-linear) imperfections:
  - Slew rate limitations
  - Finite swing
  - Offset voltage
  - Input bias and offset currents
  - Noise and distortion

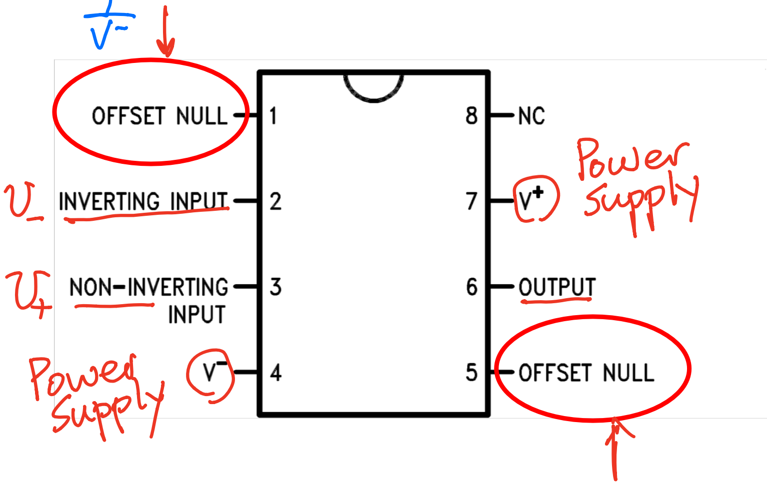
Offset Voltage

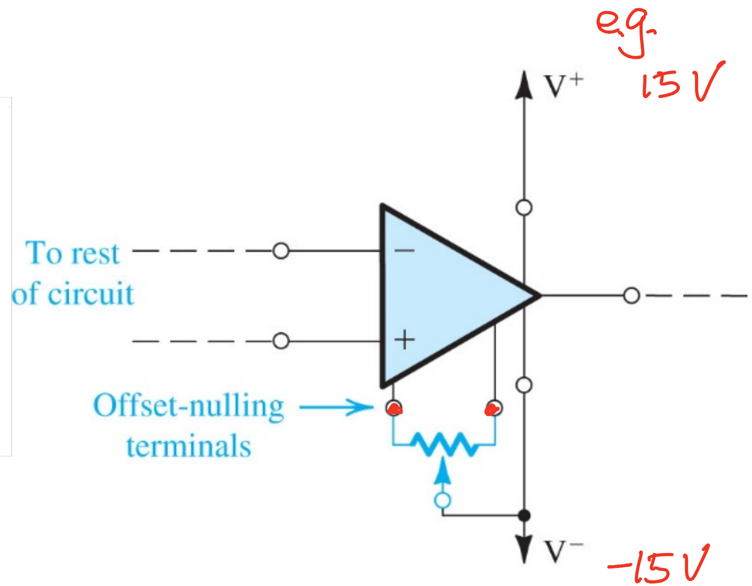


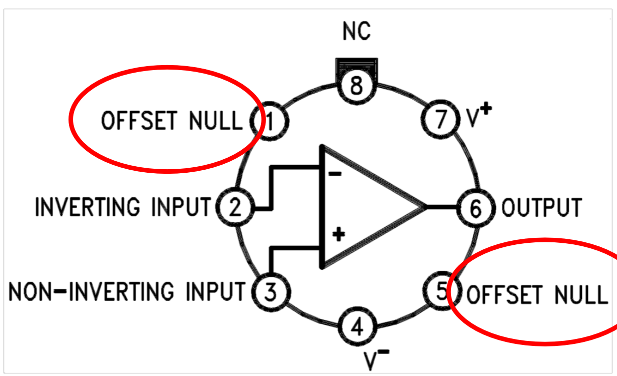


Trimming of Offset Voltage





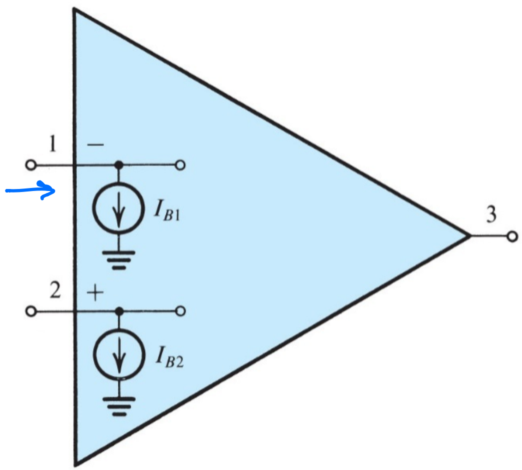




The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

Input Bias Currents and Offset Currents

BJT : Bipolar Junction Transitor



$I_{B1} \approx I_{B2} \sim 100\ nA$

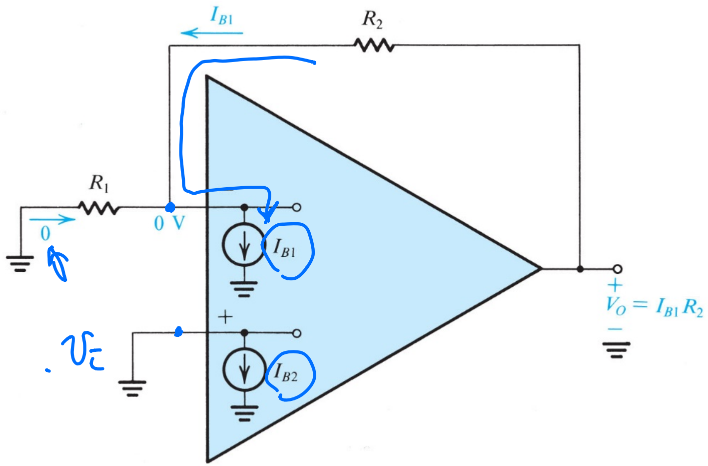
not identical

- **Some op-amps (bipolar) have input bias currents that need to flow for the op-amp to function properly**
- **They are typically very small, ~ 100 nA, but may differ slightly (by 10 nA)**

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

$$I_{OS} = |I_{B1} - I_{B2}| \sim 10\ nA$$

Effect of Input Bias Current in Amplifier Circuit



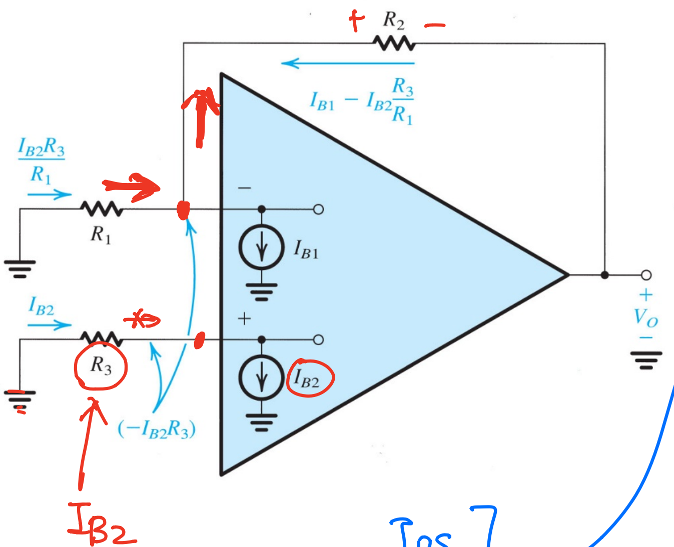
In the absence of input voltage, the output should be zero for ideal Op Amp. However, with non-zero I_B,

$$V_O = I_{B1}R_2 \approx I_B R_2$$

Ideal, $v_i = 0$, $V_o = 0$

$v_- = 0$, $I_{B1} = \frac{V_o - 0}{R_2} \Rightarrow V_o = I_{B1} \cdot R_2$

Reducing the Effect of Input Bias Currents



$$V_+ = 0 - I_{B2}\cdot R_3 = -I_{B2}\cdot R_3$$

$$V_o = -I_{B2}\cdot R_3 + \underbrace{\left(\frac{0-(-I_{B2}R_3)}{R_1} - I_{B1}\right)}_{\text{current } R_2}\cdot R_2$$

Let $I_{B1} = I_{B2}$

$$V_o = I_B\cdot\left(R_2 - R_3\cdot\left(1+\frac{R_2}{R_1}\right)\right)$$

Set $R_3 = \dfrac{R_2}{1+\frac{R_2}{R_1}} = \dfrac{R_1R_2}{R_1+R_2} = R_1 /\!/ R_2$

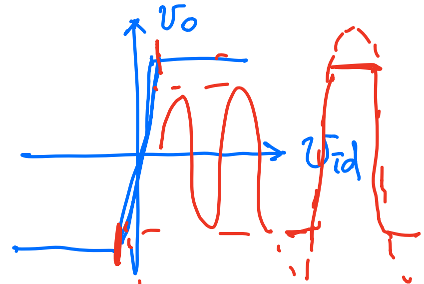
$\Rightarrow V_o = 0$

$$I_{B1} = I_B + \frac{I_{OS}}{2}$$
$$I_{B2} = I_B - \frac{I_{OS}}{2}$$

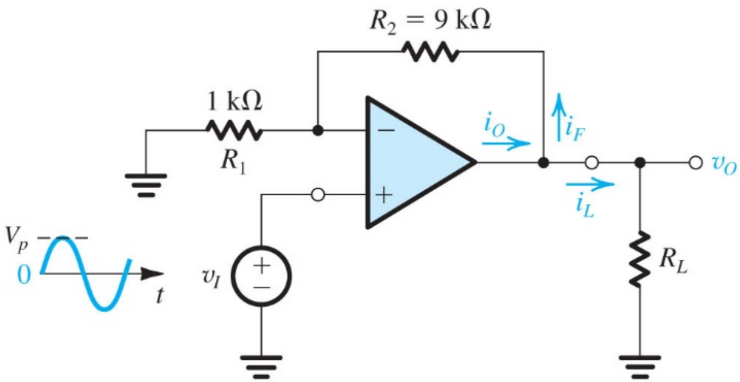
$$V_o = I_{OS}R_2$$

↑ 10% of I_B

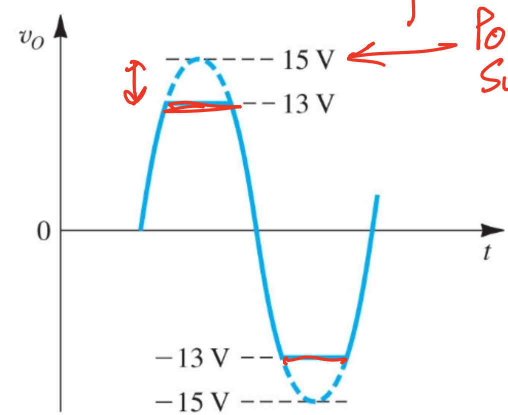
Output Saturation



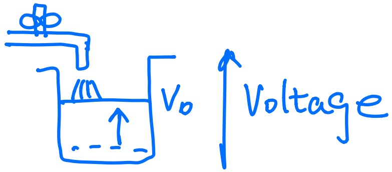
- **The output voltage swing is limited by**
  1. **Saturation voltage (usually a volt or two lower than power supply voltage)**
  2. **Maximum output current (in case of small load resistance)**
- **Output waveform appears to be "clipped" when either condition happens**



(a)



(b)

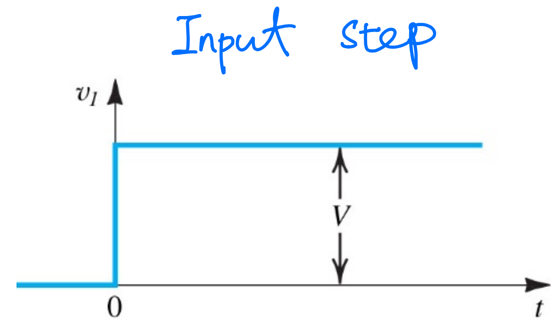


Slew Rate

Amplifier output is limited by "slew rate":
maxium rate of change possible at output

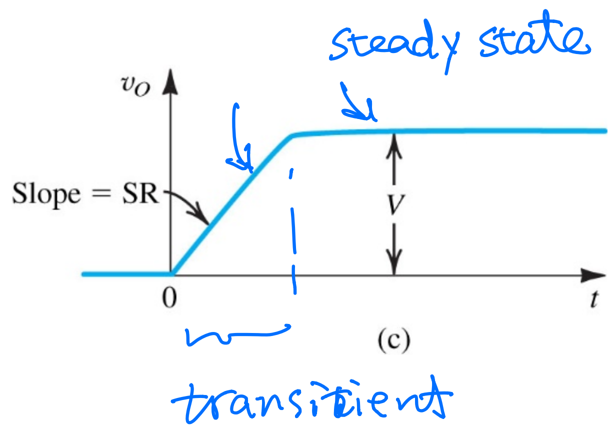
$$SR = \left.\frac{dv_o}{dt}\right|_{max}$$

SR is specified in datasheet in [V/μs]



(b)

**Output not able to follow input;
Slope limited by SR**

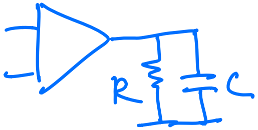


(c)

Note

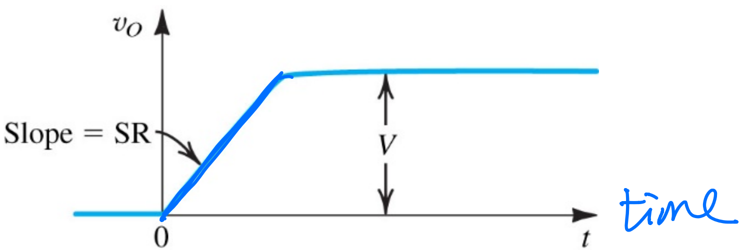
SR limit is different from bandwidth limit:

- Limited bandwidth is a linear phenomenon, it does not change the shape of input sinusoid
- SR limitation can cause nonlinear distortion to input sinusoidal signal

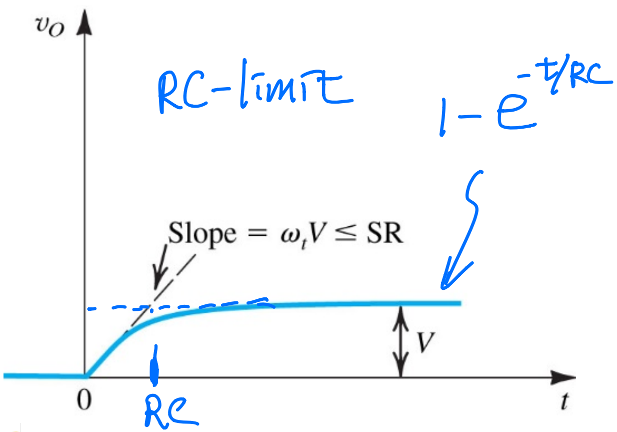


Comparison of Slew Rate and Bandwidth Limits

For step function input waveform, both SR and bandwidth limits cause the output to rise with a finite slope, but there is an important difference:

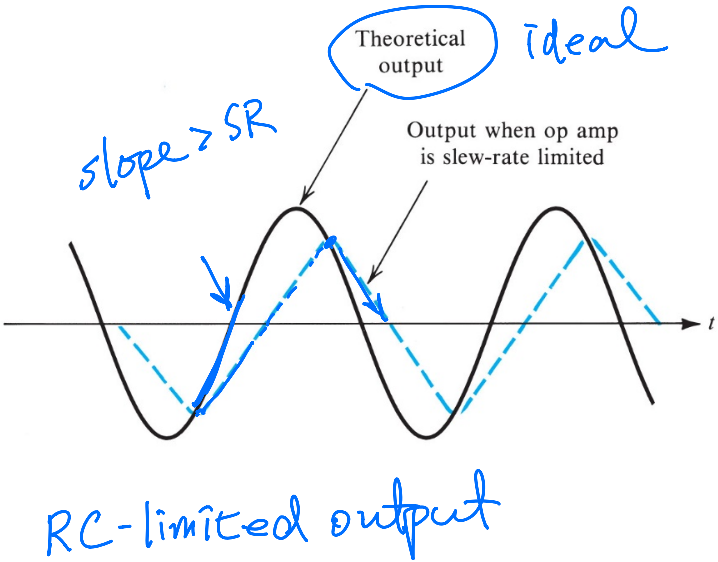


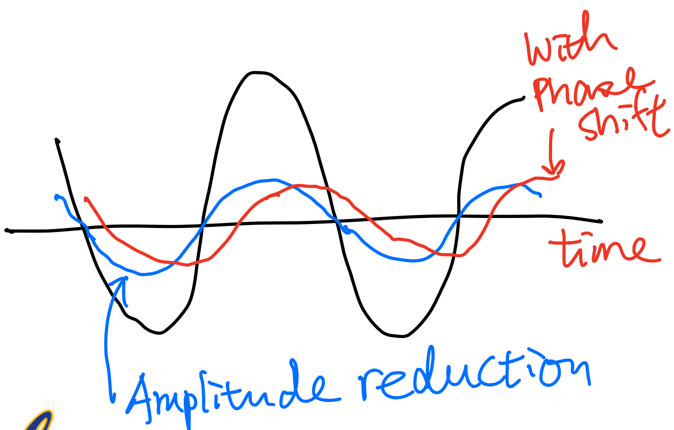
Slew rate limited output:
Slope = SR



Bandwidth limited output:
Slope = $\omega_t V$ < SR
(V is the steady state output voltage)

Full-Power Bandwidth





For ideal sinusoidal output

$$v_o = V_o \sin \omega t$$

Rate of change cannot exceed SR:

$$\frac{dv_o}{dt} = V_o \omega \cdot \cos \omega t \leq \text{SR}$$

Full-power bandwidth:

The frequency at which SR-limited distortion starts to occur for an output sinusoid with maximum rated output voltage, V_{omax},

$$\omega_M V_{omax} = SR$$

$$f_M = \frac{SR}{2\pi V_{omax}}$$

Op Amp Catalog (ti.com)

https://www.ti.com/amplifier-circuit/op-amps/products.html#

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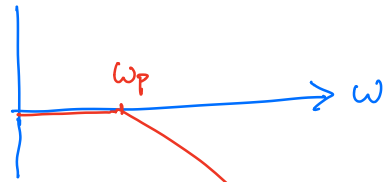
- Number of Channels (#): ≥ 1 ≤ 4 — 1468 total parts
- Total Supply Voltage (Min) (+5V=5, +/-5V=10): ≥ 0.9 ≤ 40 — 1468 total parts
- Total Supply Voltage (Max) (+5V=5, +/-5V=10): ≥ 3 ≤ 105 — 1468 total parts
- GBW (Typ) (MHz)
- Slew Rate (Typ) (V/us)
- Rail-to-Rail
- Vos (Offset Voltage @ 25C) (Max) (mV)
- Iq per channel (Typ) (mA)
- Rating

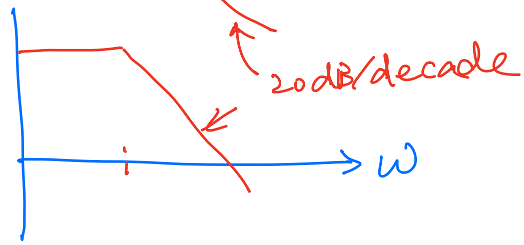
1468 total parts | Email | Download to Excel

Compare	Part Number	Number of Channels (#)	Total Supply Voltage (Min) (+5V=5, +/-5V=10)	Total Supply Voltage (Max) (+5V=5, +/-5V=10)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/us)	Rail-to-Rail	Vos (Offset Voltage @ 25C) (Max) (mV)	Iq per channel (Typ) (mA)	Rating	Operating Temperature Range (C)	Package Group	Approx. Price (US$)
☐	ACF2101 - Low Noise, Dual Switched Integrator	2	14.5	36	2	3	No	2	15.5	Catalog	-40 to 125	SOIC	21.06 | 1ku
☐	AFE030 - Powerline Communications Analog Front-End	1	7	26	0.67	19	No		40	Catalog	-40 to 125	VQFN	1.75 | 1ku
☐	AFE031 - Powerline Communications Analog Front End	1	7	26	0.67	19	No		49	Catalog	-40 to 125	VQFN	2.00 | 1ku
☐	AFE032 - Power Line Communications Analog Front End	1	7	24	3.8	75	No		78	Catalog	-40 to 125	VQFN	3.50 | 1ku
☐	ALM2402-Q1 - Dual Opamp with High Current Output	2	5	16	0.6	0.17	No	15	5	Automotive	-40 to 125	HTSSOP, SON	1.29 | 1ku
☐	BUF602 - High Speed, Closed Loop Buffer	1	2.8	12.6	1000	8000	No	30		Catalog	-45 to 85	SOIC, SOT-23	0.93 | 1ku
☐	BUF634 - 250mA High-Speed Buffer	1	5	36	180	2000	No	100	1.5	Catalog	-40 to 125	DDPAK/TO-263, PDIP, SOIC, TO-220	3.50 | 1ku
☐	DRV2700 - DRV2700 High Voltage Driver with Integrated Boost Converter	1	15	105	0.550	0.6		25	13	Catalog	-40 to 85	QFN	4.95 | 1ku
☐	ICL7652 - Precision Chopper-Stabilized Operational Amplifier	1	7	36	1.9	2.8	In to V-, Out	0.005	1.5	Catalog	0 to 70	PDIP	2.91 | 1ku
☐	LF147 - Wide Bandwidth Quad JFET Input Operational Amplifiers - Hi-Rel	4	5	44	4	13	In to V+	5	1.8	Military	-55 to 125	CDIP	
☐	LF156 - JFET Input Operational	1	10	44	5	12	In	2	5	Military	-55 to 125	TO-99	

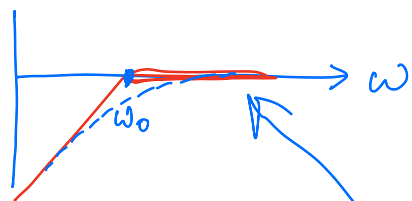
LPF $\quad \dfrac{1}{\left(1+j\frac{\omega}{\omega_p}\right)}$



LP Amplifier $\quad \dfrac{A_0}{1+j\frac{\omega}{\omega_p}}$



HPF $\quad H(\omega)=\dfrac{1}{1+\frac{\omega_0}{j\omega}}$



$\omega \ll \omega_0$

$H(\omega) \rightarrow \dfrac{1}{\frac{\omega_0}{j\omega}} = \dfrac{j\omega}{\omega_0} \propto \omega$

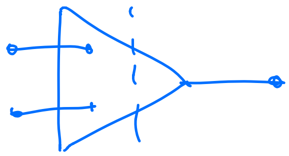
$\omega \gg \omega_0$

$H(\omega) \rightarrow 1 = 0\,dB$

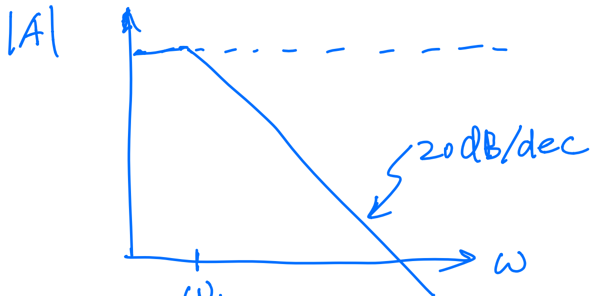
$\omega = \omega_0,\quad H(\omega) = \dfrac{1}{1+j} \Rightarrow \begin{array}{l} -3dB \\ \angle = -45^\circ \end{array}$

$\dfrac{j\omega}{j\omega+\omega_0} = \dfrac{s}{s+\omega_0}$

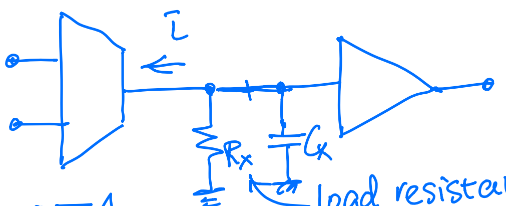
$s = j\omega$



$$A \rightarrow A(j\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_b}}$$



Buffer, Low R_o



load resistance of OTA + Input resistance of buffer

OTA

$$i = G_m(v_+ - v_-) = G_m v_{id}$$